# Precision Voltage Supervisory Circuit With Watchdog Timer and 16K I²C Memory

3 and 5 Volt Systems

## FEATURES

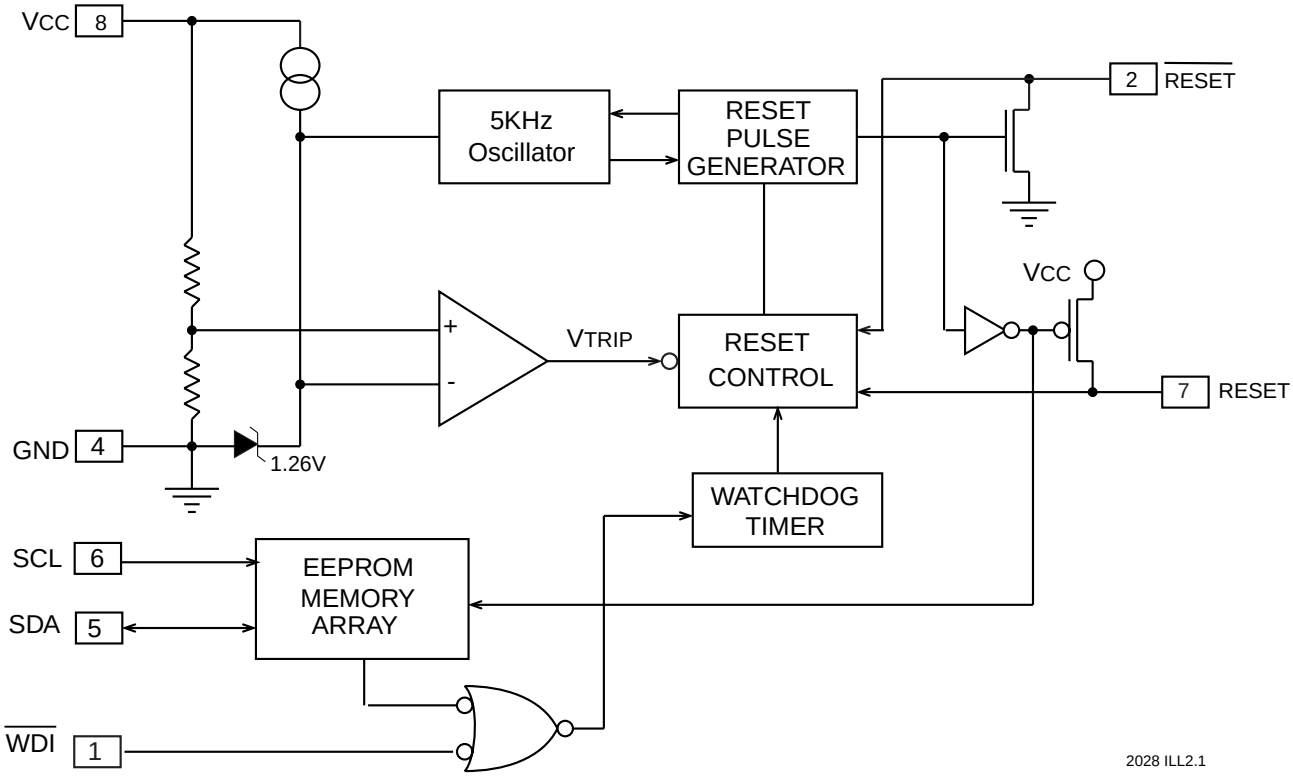
- **Precision Voltage Monitor**
  - **Automatic $V_{CC}$ Supply Monitor**
    - **Complementary reset outputs for complex microcontroller systems**
    - **Integrated memory write lockout function**
    - **No external components required**
- **Watchdog Timer**
  - **Nominal 1.6 second Timeout**
- **Memory Internally Organized 2K X 8**
  - **Two Wire Serial Interface (I²C™)**
- **High Reliability**
  - **Endurance: 1,000,000 erase/write cycles**
  - **Data retention: 100 years**
- **8-Pin PDIP or SOIC Packages**

## OVERVIEW

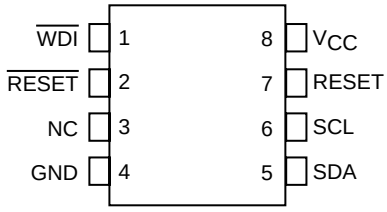
The SMS2916 is a power supervisory circuit that monitors $V_{CC}$ (either in a 5V system or 3V system) and will generate complementary reset outputs. The reset pins also act as I/Os and may be used for signal conditioning. The SMS2916 also has an on-board watchdog timer that has a nominal time out period of 1.6 seconds.

The SMS2916 integrates a 16K-bit nonvolatile serial memory. It features the industry standard I²C serial interface allowing quick implementation in an end-users' system.

## BLOCK DIAGRAM



## PIN CONFIGURATIONS

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## PIN NAMES

| Symbol | Pin | Description |
|---|---|---|
| $\overline{WDI}$ | 1 | Watchdog Input /a high to low transition will clear the watchdog timer |
| $\overline{RESET}$ | 2 | Active Low RESET Input/Output |
| NC | 3 | No Connect, tie to ground or leave open |
| GND | 4 | Analog and Digital Ground |
| SDA | 5 | Serial Memory Input/ Output data line |
| SCL | 6 | Serial Memory clock input |
| RESET | 7 | Active High RESET Input/ Output |
| $V_{CC}$ | 8 | Supply Voltage |

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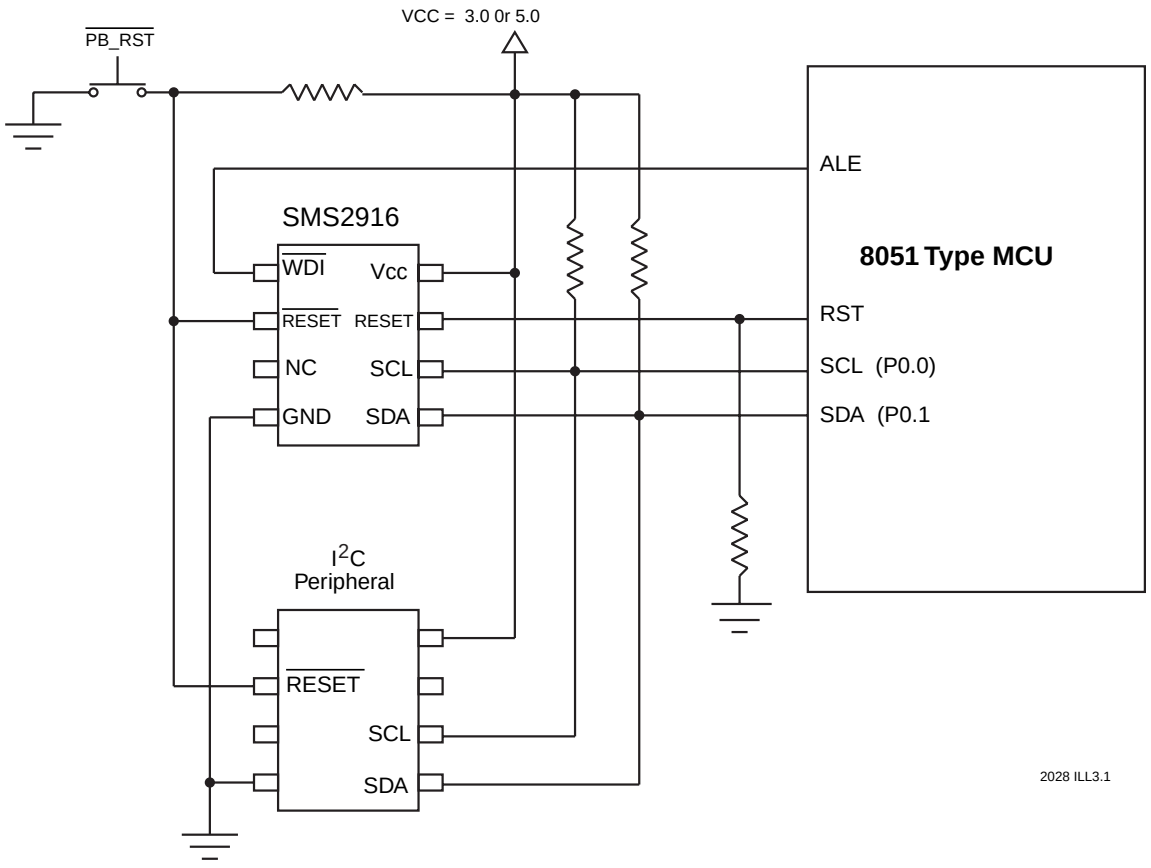


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**FIGURE 1. TYPICAL APPLICATION USING DUAL RESET FUNCTION AND WATCHDOG TIMER**

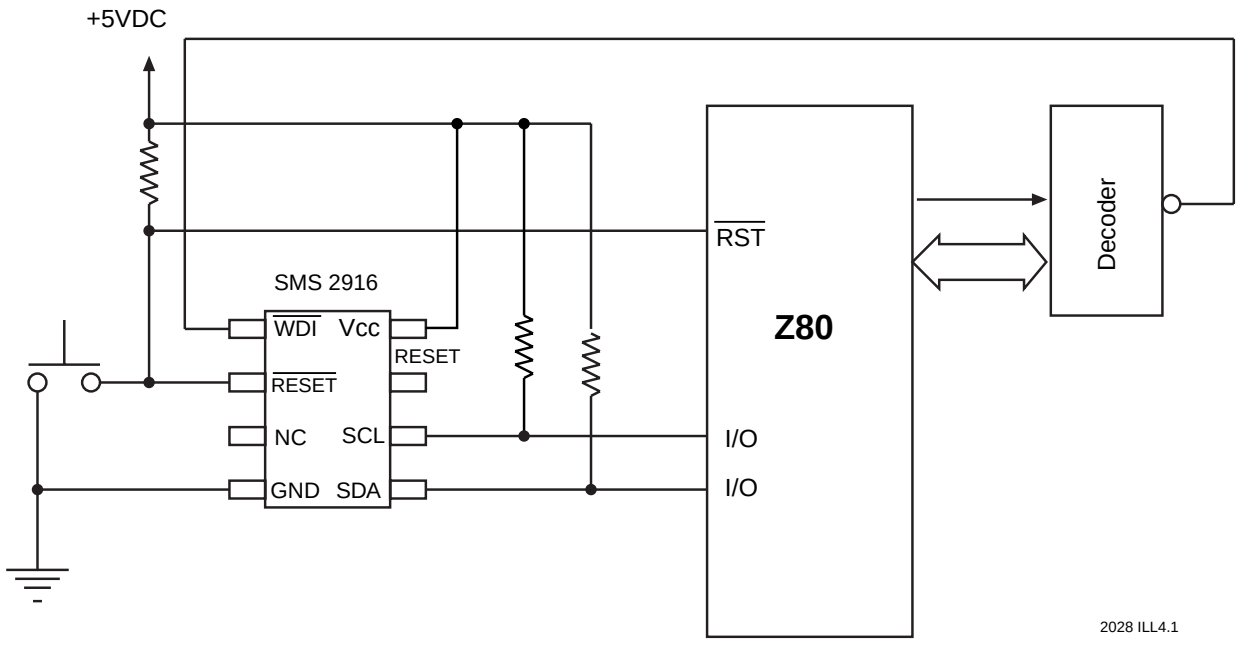


**FIGURE 2. TYPICAL APPLICATION CONFIGURATION USING SYSTEM DECODE LOGIC TO RESET WDI**

**CAPACITANCE**

$T_A$ = 25°C, f = 100KHz

| Symbol | Parameter | Max | Units |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 5 | pF |
| $L_{OUT}$ | Output Capacitance | 8 | pF |

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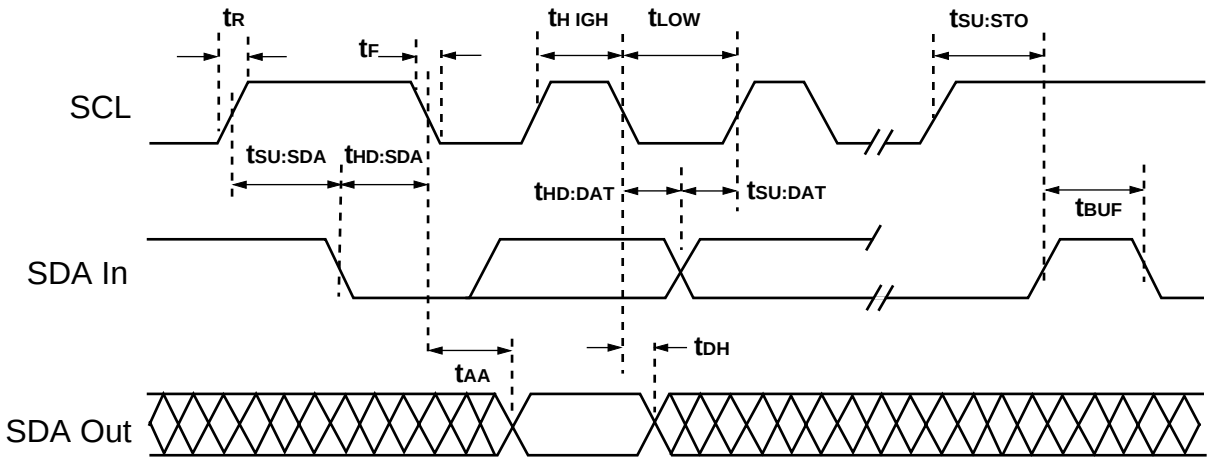


**FIGURE 3. BUS TIMING**

## ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3V to $V_{CC}$+0.3V
ESD Voltage (JEDEC method) ..... 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temperature | Min | Max |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |

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## DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

| Symbol | Parameter | Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Supply Current (CMOS) | SCL = CMOS Levels @ 100KHz<br>SDA = Open<br>All other inputs = GND or $V_{CC}$ | $V_{CC}$ =5.5V | | 3 | mA |
| | | | $V_{CC}$ =3.3V | | 2 | mA |
| $I_{SB}$ | Standby Current (CMOS) | SCL = SDA = $V_{CC}$<br>All other inputs = GND | $V_{CC}$ =5.5V | | 50 | µA |
| | | | $V_{CC}$ =3.3V | | 25 | µA |
| $I_{LI}$ | Input Leakage | $V_{IN}$ = 0 To $V_{CC}$ | | | 10 | µA |
| $I_{LO}$ | Output Leakage | $V_{OUT}$ = 0 To $V_{CC}$ | | | 10 | µA |
| $V_{IL}$ | Input Low Voltage | S0, S1, S2, SCL, SDA, $\overline{\text{RESET}}$ | | | 0.3x$V_{CC}$ | V |
| $V_{IH}$ | Input High Voltage | S0, S1, S2, SCL, SDA, RESET | | 0.7x$V_{CC}$ | | V |
| $V_{OL}$ | Output Low Voltage | $I_{OL}$ = 3mA SDA | | | 0.4 | V |

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## AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions unless otherwise specified)

| | | | 2.7V to 4.5V | | 4.5V to 5.5V | | |
|---|---|---|---|---|---|---|---|
| Symbol | Parameter | Conditions | Min | Max | Min | Max | Units |
| $f_{SCL}$ | SCL Clock Frequency | | 0 | 100 | | 400 | KHz |
| $t_{LOW}$ | Clock Low Period | | 4.7 | | 1.3 | | µs |
| $t_{HIGH}$ | Clock High Period | | 4.0 | | 0.6 | | µs |
| $t_{BUF}$ | Bus Free Time | Before New Transmission | 4.7 | | 1.3 | | µs |
| $t_{SU:STA}$ | Start Condition Setup Time | | 4.7 | | 0.6 | | µs |
| $t_{HD:STA}$ | Start Condition Hold Time | | 4.0 | | 0.6 | | µs |
| $t_{SU:STO}$ | Stop Condition Setup Time | | 4.7 | | 0.6 | | µs |
| $t_{AA}$ | Clock to Output | SCL Low to SDA Data Out Valid | 0.3 | 3.5 | 0.2 | 0.9 | µs |
| $t_{DH}$ | Data Out Hold Time | SCL Low to SDA Data Out Change | 0.3 | | 0.2 | | µs |
| $t_R$ | SCL and SDA Rise Time | | | 1000 | | 300 | ns |
| $t_F$ | SCL and SDA Fall Time | | | 300 | | 300 | ns |
| $t_{SU:DAT}$ | Data In Setup Time | | 250 | | 100 | | ns |
| $t_{HD:DAT}$ | Data In Hold Time | | 0 | | 0 | | ns |
| $T_I$ | Noise Spike Width @ SCL, SDA Inputs | Noise Suppression Time Constant | | 100 | | 100 | ns |
| $t_{WR}$ | Write Cycle Time | | | 10 | | 10 | ms |

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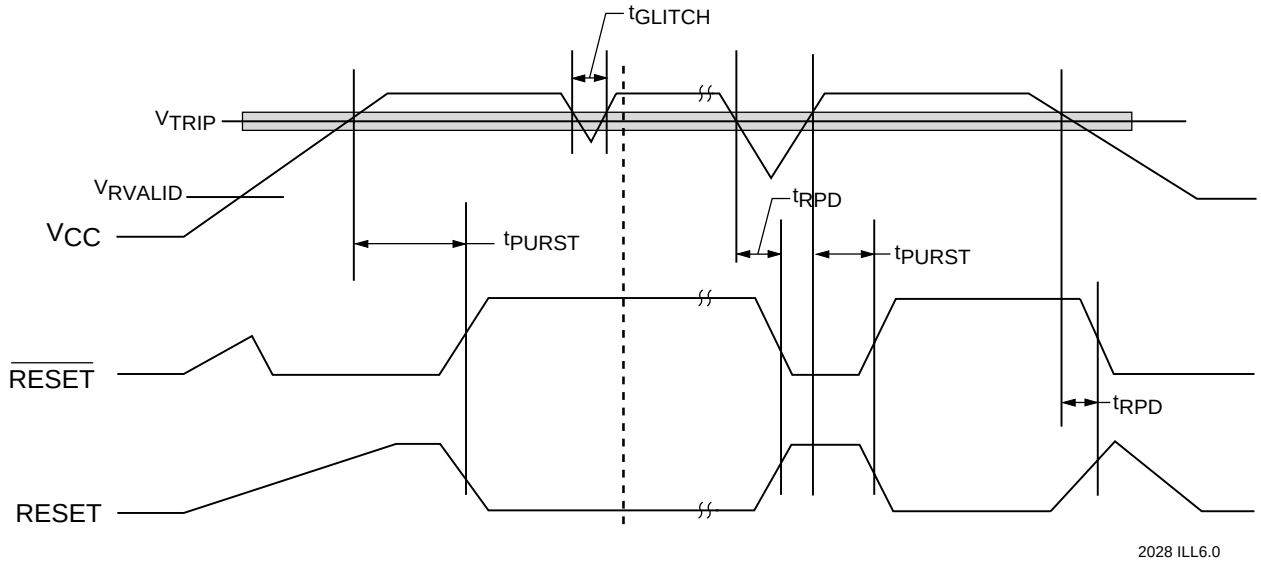


**FIGURE 4. RESET OUTPUT TIMING**

## RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

$T_A$ = -40°C to +85°C

| | | SMS2916-2.7 | | SMS2916–A | | SMS2916–B | | |
|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $V_{TRIP}$ | Reset Trip Point | 2.55 | 2.7 | 4.25 | 4.5 | 4.5 | 4.75 | V |
| $t_{PURST}$ | Power-Up Reset Timeout | 130 | 270 | 130 | 270 | 130 | 270 | ms |
| $t_{RPD}$ | $V_{TRIP}$ to RESET Output Delay | | 5 | | 5 | | 5 | µs |
| $V_{RVALID}$ | $\overline{\text{RESET}}$ Output Valid | 1 | | 1 | | 1 | | V |
| $t_{GLITCH}$ | Glitch Reject Pulse Width | | 30 | | 30 | | 30 | ns |
| $V_{OLRS}$ | $\overline{\text{RESET}}$ Output Low Voltage $I_{OL}$= 1mA | | 0.4 | | 0.4 | | 0.4 | V |
| $V_{OHRS}$ | RESET Output High Voltage $I_{OH}$ = 800 µA | $V_{CC}$-.75 | | $V_{CC}$-.75 | | $V_{CC}$-.75 | | V |

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## PIN DESCRIPTIONS

**Serial Clock (SCL)** - The SCL input is used to clock data into and out of the device. In the WRITE mode, data must remain stable while SCL is HIGH. In the READ mode, data is clocked out on the falling edge of SCL.

**Serial Data (SDA)** - The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

**$\overline{\text{RESET}}$** - $\overline{\text{RESET}}$ is an active low output. Whenever $V_{CC}$ is below $V_{TRIP}$ the SMS2916 will drive the $\overline{\text{RESET}}$ pin to ground. The $\overline{\text{RESET}}$ pin is an I/O and can be used as a reset input. Refer to Figure 1 as an example use of this pin as a push button switch debounce circuit. It should be noted this is an open drain output and an external pull-up resistor tied to $V_{CC}$ is needed for proper operation.

**RESET** — RESET is an active high output. Whenever $V_{CC}$ is below $V_{TRIP}$ the SMS2916 will drive the RESET pin to the $V_{CC}$ rail. The RESET pin is an I/O and can be used as a reset input. It should be noted this is an open drain output and an external pull-down resistor tied to ground is needed for proper operation.

**$\overline{\text{WDI}}$** - The $\overline{\text{WDI}}$ input is used as a hardware method of clearing the watchdog timer. A high to low transition on this pin will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

## ENDURANCE AND DATA RETENTION

The SMS2916 is designed for applications requiring 1,000,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 1,000,000 erase/write cycles.

### Reset Controller Description

The SMS2916 provides a precision RESET controller that ensures correct system operation during brown-out and power-up/-down conditions. It is configured with two open drain RESET outputs; pin 7 is an active high output and pin 2 is an active low output.

During power-up, the RESET outputs remain active until $V_{CC}$ reaches the $V_{TRIP}$ threshold and will continue driving the outputs for approximately 200ms after reaching $V_{TRIP}$. The RESET outputs will be valid so long as $V_{CC}$ is > 1.0V. During power-down, the RESET outputs will begin driving active when $V_{CC}$ falls below $V_{TRIP}$.

The RESET pins are I/Os; therefore, the SMS2916 can act as a signal conditioning circuit for an externally applied reset. The inputs are edge triggered; that is, the RESET input will initiate a reset timeout after detecting a low to high transition and the $\overline{\text{RESET}}$ input will initiate a reset timeout after detecting a high to low transition. Refer to the applications Information section for more details on device operation as a reset conditioning circuit.

## WATCHDOG TIMER OPERATION

The SMS2916 has a watchdog timer with a nominal timeout period of 1.6 seconds. Whenever the watchdog times out it will generate a reset output on both $\overline{\text{RESET}}$ and RESET. There are two methods of clearing the watchdog timer; the first is through the use of software, and the second is by strobing the WDI input pin.

### Software Method

The watchdog timer will clear to t0 whenever the SMS2916 issues an ACKnowledge. Therefore, the host system will need to issue a start condition, followed by a valid address and command. It can be a normal command as in the sequence of reading or writing to the memory, or it can be a dummy command issued solely for the purpose of resetting the watchdog timer. Refer to Figure 12 for detailed sequence of operations.

The watchdog timer will be held in the cleared state during power-on while $V_{CC}$ is less than $V_{TRIP}$. Once $V_{CC}$ exceeds $V_{TRIP}$ the watchdog will continue to be held in a cleared state for the duration of $t_{PURST}$. After $t_{PURST}$, the timer will be released and begin counting.

If either reset input is asserted the watchdog timer will be cleared and remain in the reset condition until either $t_{PURST}$ has expired or the reset input is released, whichever is longer.

If the watchdog times out and no action is taken by the host the SMS2916 will drive the reset outputs active for the duration of $t_{PURST}$ at which point it will release the outputs and clear the watchdog timer again and release it to begin a new count. Refer to Figure 13 for detailed sequence of operations.

### Hardware Method

A high to low transition on $\overline{\text{WDI}}$ will clear the watchdog timer. If a transition is not detected within 1.6 seconds the watchdog will time out and force the reset outputs active.

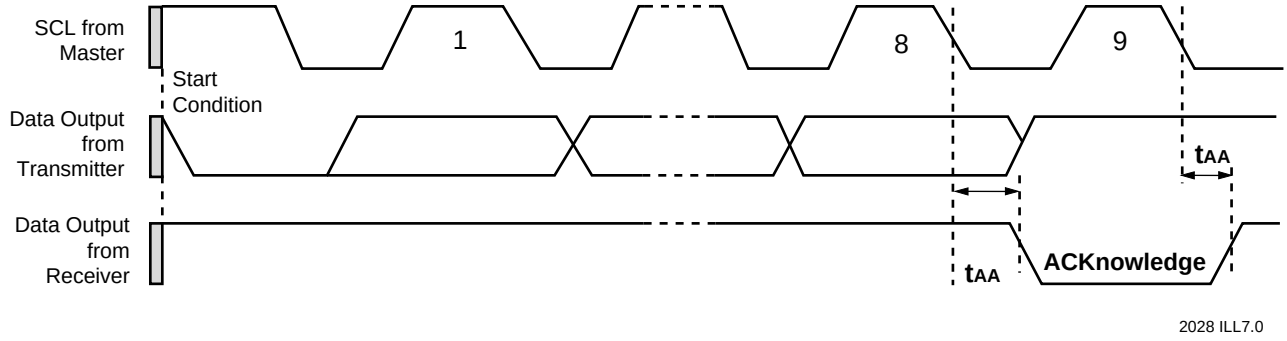



**FIGURE 5. ACKNOWLEDGE RESPONSE FROM RECEIVER**

## CHARACTERISTICS OF THE I²C BUS

### General Description

The I²C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are: a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

### Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition.

### START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the “START” condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the “STOP” condition .

## DEVICE OPERATION

The SMS2916 is a 16K-bit serial E²PROM. The device supports the I²C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a “transmitter” and any device which receives data as a “receiver.” The device controlling data transmission is called the “master” and the controlled device is called the “slave.” In all cases, the SMS2916 will be a “slave” device, since it never initiates any data transfers.

### Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 5).

The SMS2916 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the SMS2916 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode, the SMS2916 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the SMS2916 will continue to transmit data. If an ACKnowledge is not detected, the SMS2916 will terminate further data transmissions and awaits a STOP condition before returning to the standby power mode.

### Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 6). For the SMS2916 this is fixed as 1010[B].

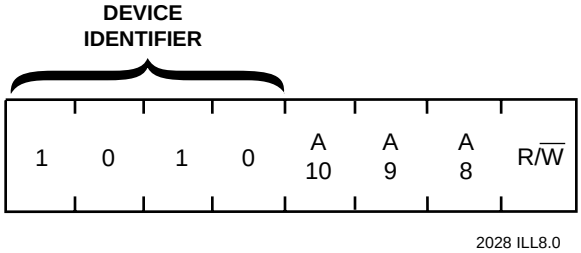



**FIGURE 6. SLAVE ADDRESS BYTE**

The next three bits are the high order address bit A8.

**Read/Write Bit**
The last bit of the data stream defines the operation to be performed. When set to “1,” a read operation is selected; when set to “0,” a write operation is selected.

## WRITE OPERATIONS

The SMS2916 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period ($t_{WR}$). The page write operation allows up to 16 bytes in the same page to be written during $t_{WR}$.

**Byte WRITE**
Upon receipt of both the slave address and word address, the SMS2916 responds with an ACKnowledge for each. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the SMS2916 begins the internal write cycle.

While the internal write cycle is in progress, the SMS2916 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

**Page WRITE**
The SMS2916 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more bytes of data. After the receipt of each byte, the SMS2916 will respond with an ACKnowledge.

The SMS2916 automatically increments the address for subsequent data words. After the receipt of each word, the low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than 16 bytes, prior to generating the STOP condition, the address counter will “roll over,” and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 7 for the address, ACKnowledge and data transfer sequence.

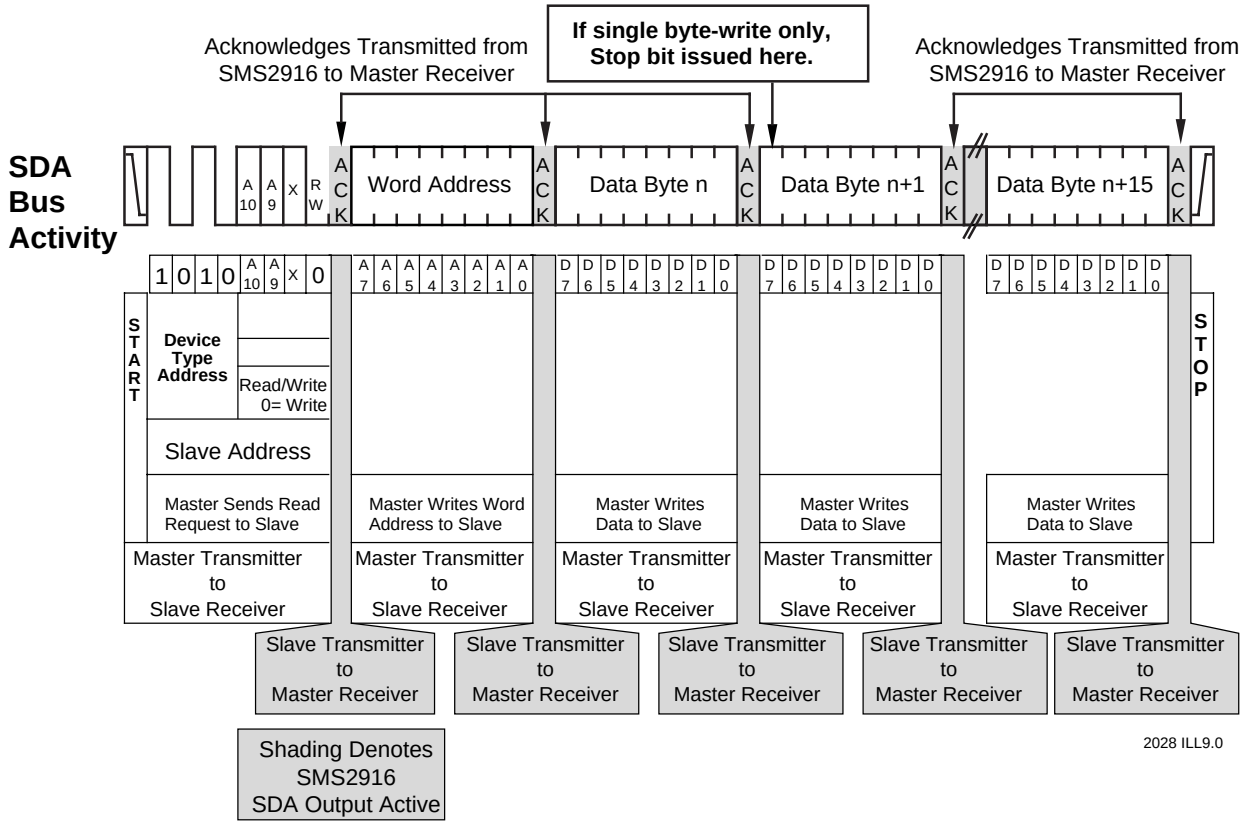



**FIGURE 7. PAGE/BYTE WRITE MODE**

### Acknowledge Polling

When the SMS2916 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 8).

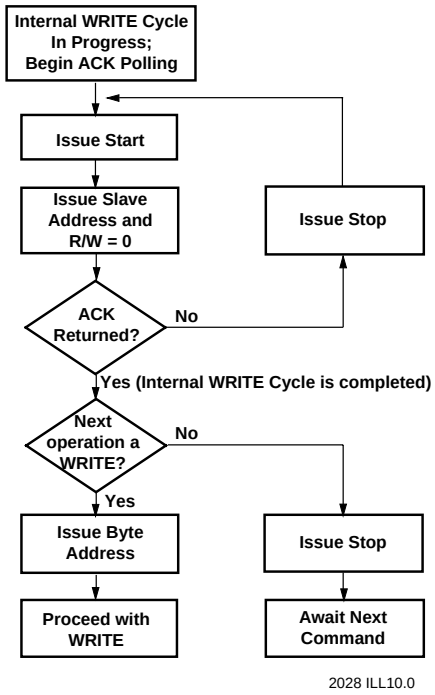



**FIGURE 8. ACKNOWLEDGE POLLING**

## READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

### Current Address Byte Read

The SMS2916 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the SMS2916 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the SMS2916 discontinues data transmission. See Figure 9 for the address acknowledge and data transfer sequence.

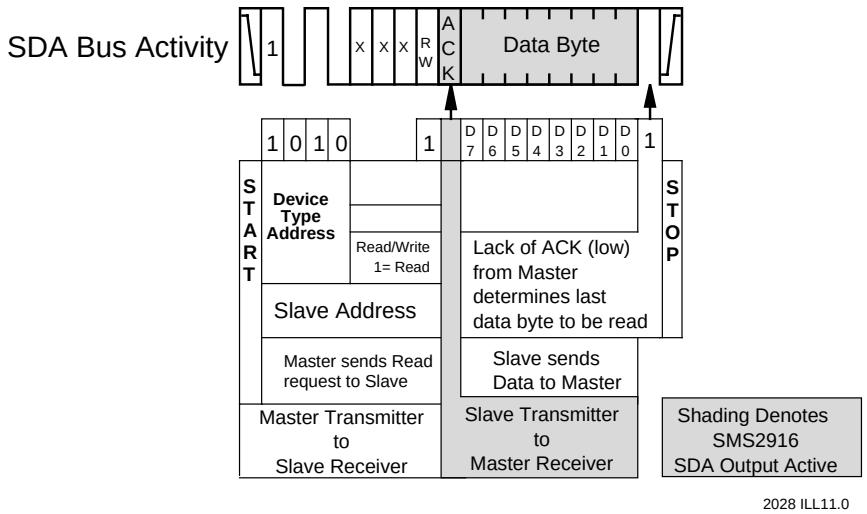



**FIGURE 9. CURRENT ADDRESS BYTE READ MODE**

**Random Address Byte Read**

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the SMS2916 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The SMS2916 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The SMS2916 discontinues data transmission and reverts to its standby power mode. See Figure 10 for the address, acknowledge and data transfer sequence.

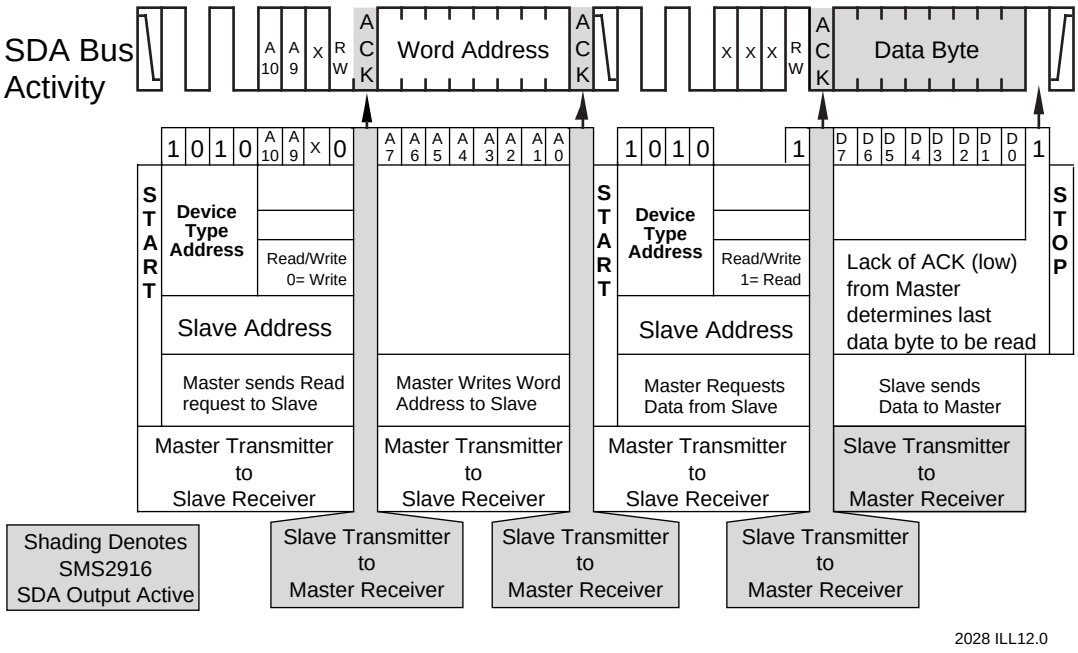



**FIGURE 10. RANDOM ADDRESS BYTE READ MODE**

**Sequential READ**

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the SMS2916. The SMS2916 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 11 for the address, acknowledge and data transfer sequence.

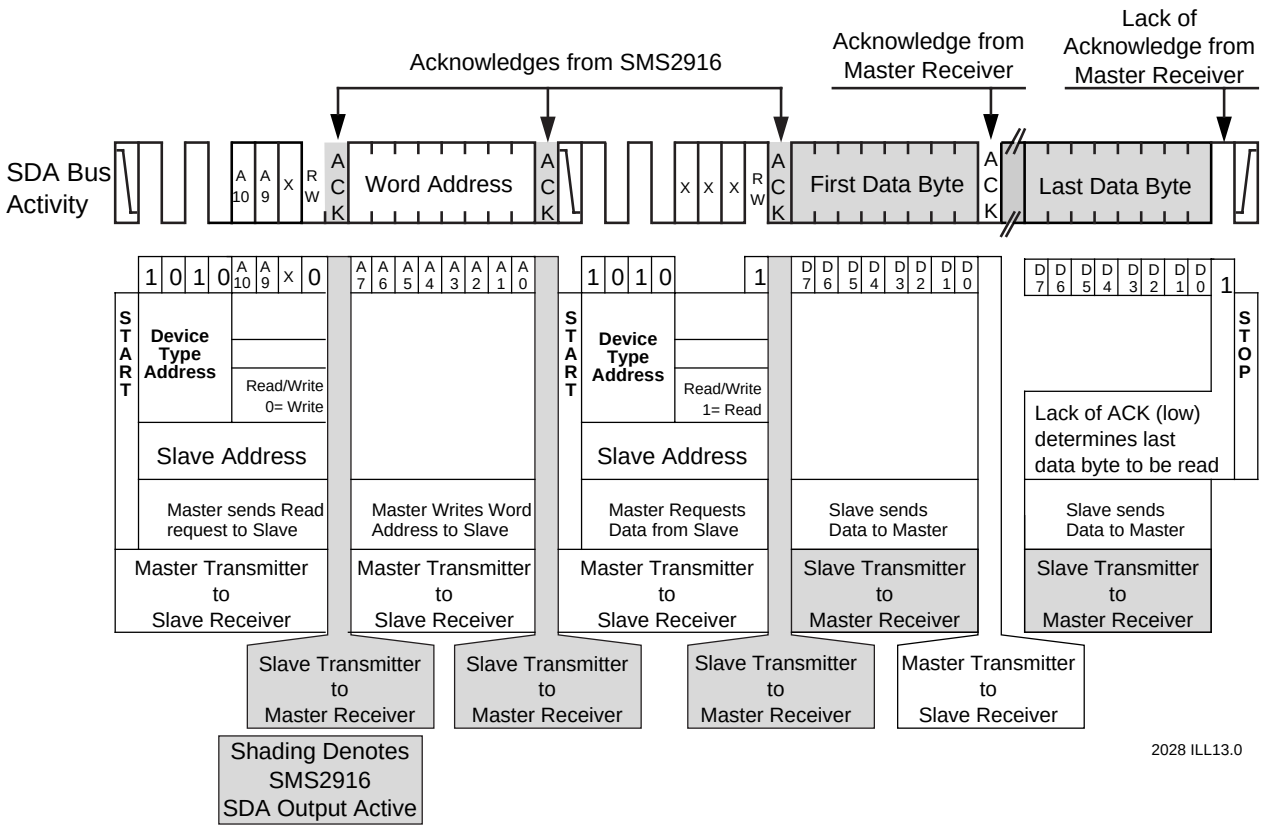



**FIGURE 11. SEQUENTIAL READ OPERATION (starting with a Random Address READ)**

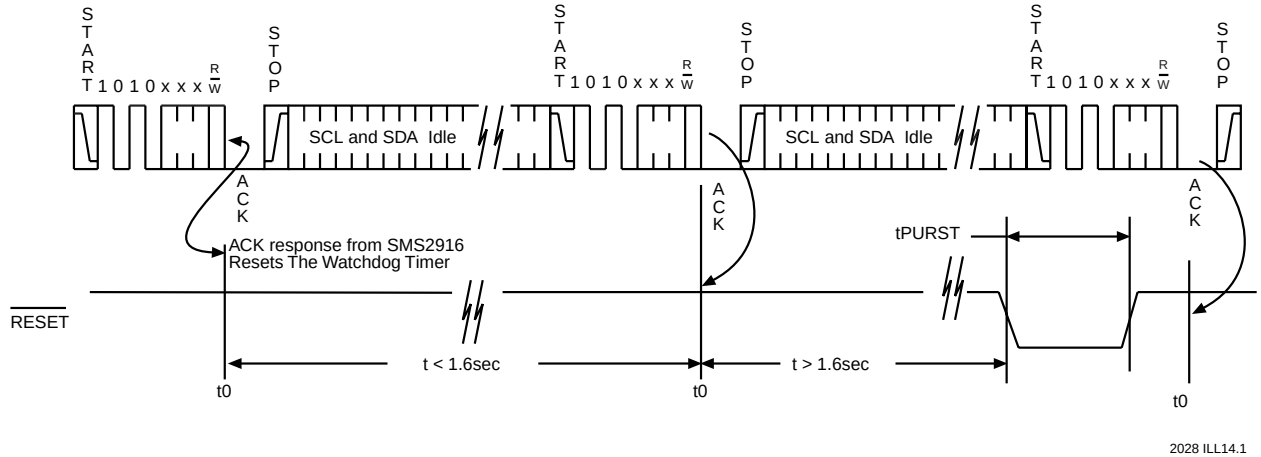



**FIGURE 12. SEQUENCE ONE**

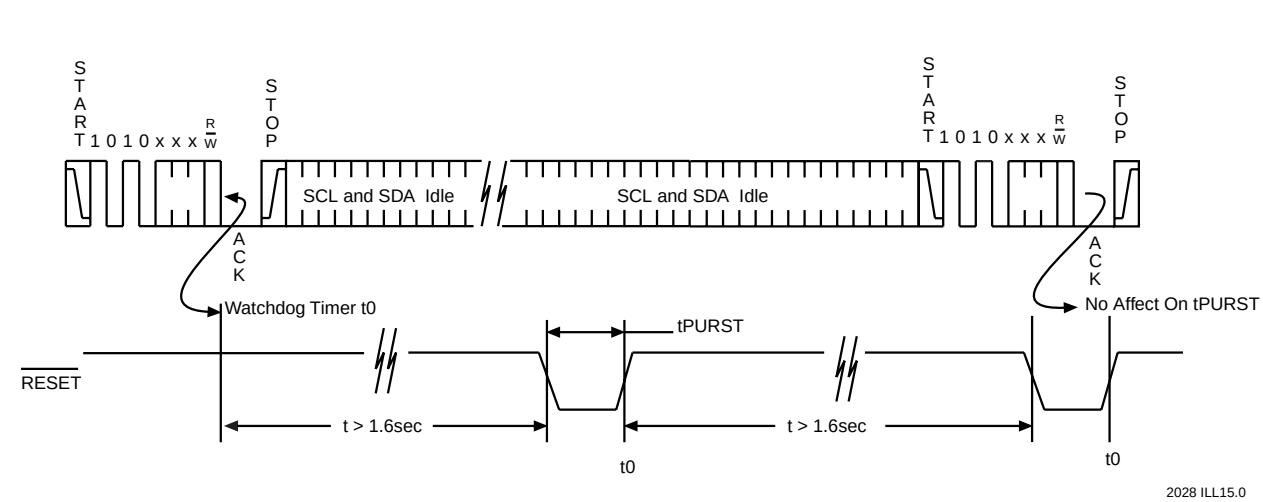
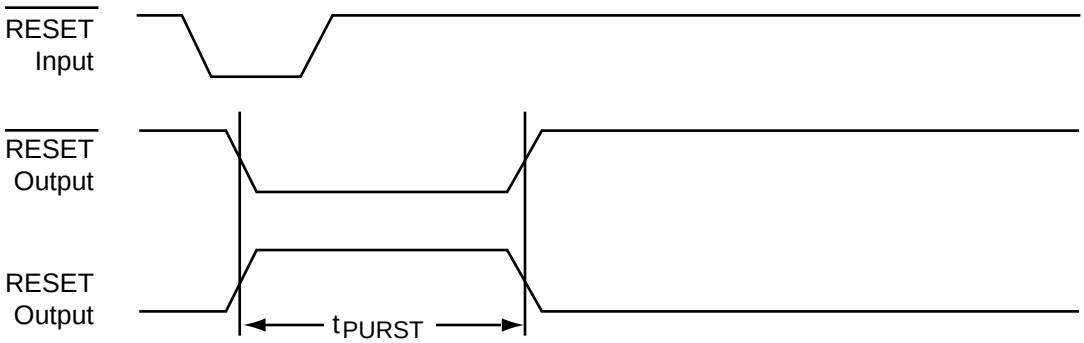



**FIGURE 13. SEQUENCE TWO**

## Applications Info

Frequently the supervisory circuit will be deployed on a PC board that provides a peripheral function to a system. Examples might be modem or network cards in a PC or a PCMCIA card in a laptop. In instances like this the peripheral card may have a requirement for a clean reset function to insure proper operation. The system may or may not provide a reset pulse of sufficient duration to clear the peripheral or to protect data stored in a nonvolatile memory.

The I/O capability of the RESET pins can provide a solution. The system's reset signal to the peripheral can be fed into the SMS2916 and it in turn can clean up the signal and provide a known entity to the peripheral's circuits. The figure below shows the basic timing characteristics under the assumption the reset input is shorter in duration than $t_{PURST}$. The same reset output affect can be attained by using the active high reset input.

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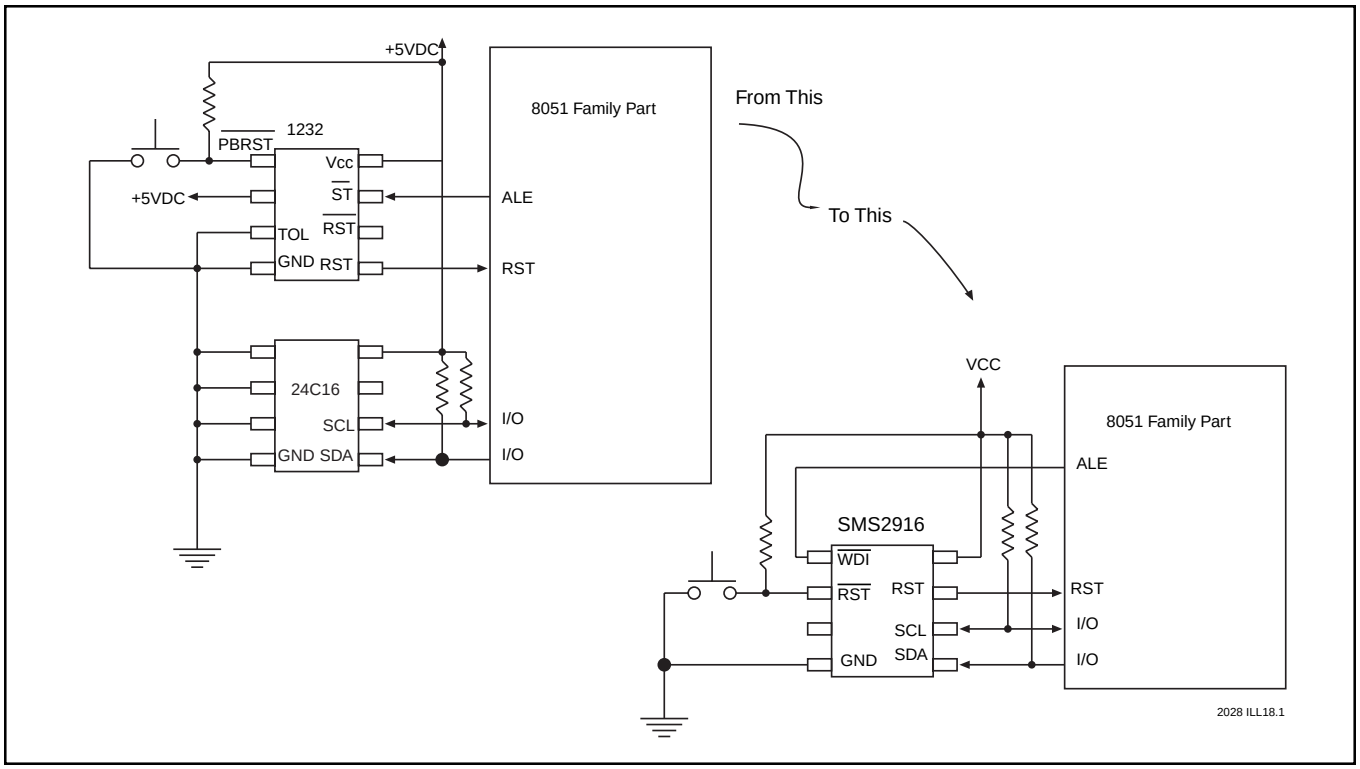
If you happen to be using one of the more common supervisory circuits like a 1232, you might consider reducing your component count such as illustrated below.

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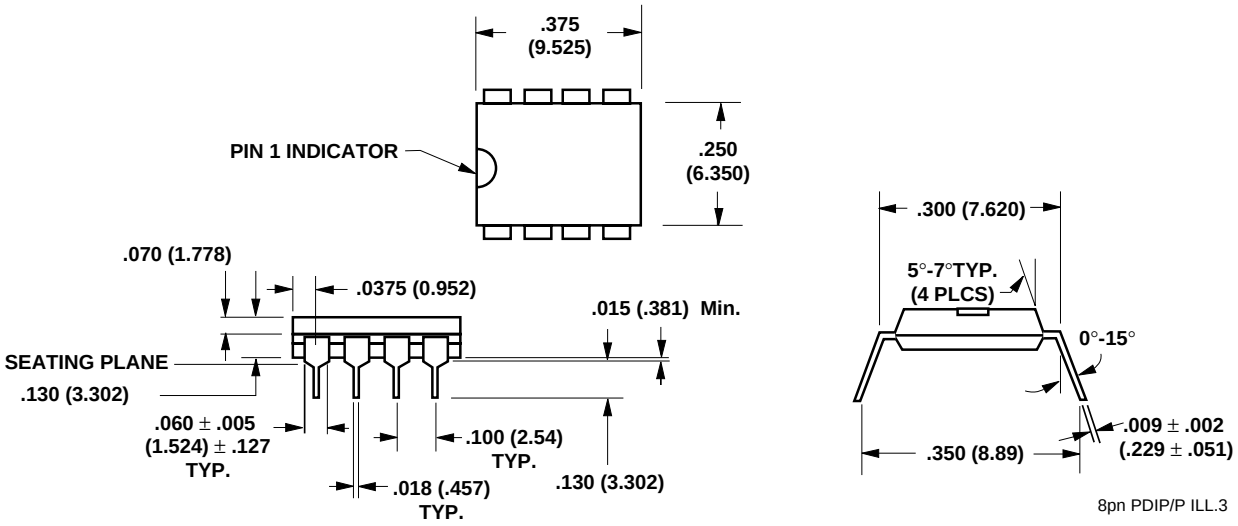
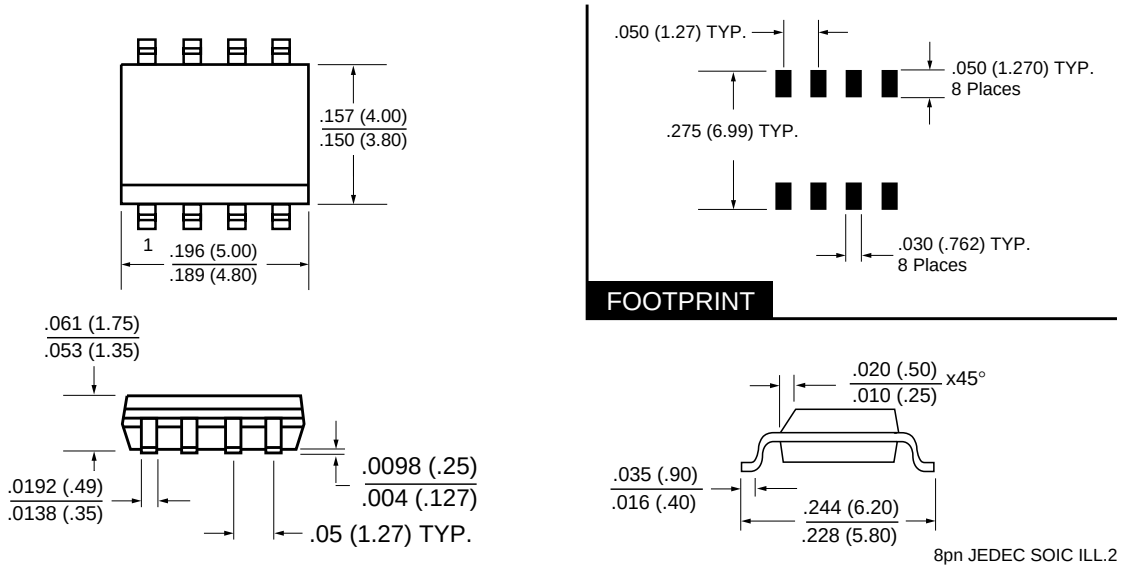
## 8 Pin PDIP (Type P) Package




8pn PDIP/P ILL.3

## 8 Pin SOIC (Type S) Package JEDEC (150 mil body width)




8pn JEDEC SOIC ILL.2

## ORDERING INFORMATION